

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the above-identified application.

Listing of Claims

1-27. Cancelled.

28. **(Currently Amended)** A method comprising:
issuing an instruction to transfer data between a memory and a processor, wherein the instruction comprises a starting address of the data to be transferred;
determining an ending address of the data to be transferred from the starting address and a memory bus [[data]] width of a memory bus coupled between the memory and the processor;
transferring the data between the memory and the processor.
29. **(Previously Presented)** The method of claim 28 further comprising:
generating an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.
30. **(Currently Amended)** The method of claim 28 wherein:
the instruction comprises a length of the data to be transferred and a stride of the data to be transferred;
wherein determining the ending address comprises:
multiplying the stride and the memory bus [[data]] width to provide a first result;
subtracting one from the length to provide a second result;
multiplying the first result and the second result to provide a third result; and
adding the third result to the starting address to provide the ending address.

31. **(Previously Presented)** The method of claim 28 further comprising:
transferring the data to be transferred between the memory and the processor via a burst transfer.
32. **(Currently Amended)** The method of claim 29 further comprising:
~~initiating a data transfer between the memory and the processor;~~
interrupting the data transfer in response to generating the address exception.
33. **(Currently Amended)** A computer readable medium comprising instructions executable by a computer system, wherein the computer system performs a method in response to executing the instructions, the method comprising:
determining an ending address of data to be transferred between a memory and a processor, wherein the ending address is determined from a starting address of the data to be transferred and a memory bus ~~[[data]]~~ width;
initiating a transfer of the data between the memory and the processor.
34. **(Previously Presented)** The computer readable medium of claim 33 wherein the method further comprises:
generating an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.
35. **(Currently Amended)** The computer readable medium of claim 34 wherein determining the ending address comprises:
multiplying a stride of the data to be transferred and the memory bus ~~[[data]]~~ width to provide a first result;
subtracting one from a length of the data to be transferred to provide a second result;
multiplying the first result and the second result to provide a third result; and
adding the third result to the starting address to provide the ending address.

36. **(Previously Presented)** The computer readable medium of claim 33 wherein the method further comprises:

transferring the data to be transferred between the memory and the processor via a burst transfer.

37. **(Currently Amended)** The computer readable medium of claim 34 wherein the method further comprises:

~~initiating a data transfer between the memory and the processor;~~

interrupting the data transfer in response to generating the address exception.

38. **(Previously Presented)** The computer readable medium of claim 37 wherein the method further comprises:

performing a burst transfer of the stream of data from the memory to the buffer of the processor, the burst transfer bypassing a data cache of the processor.

39. **(Currently Amended)** An apparatus comprising:

a memory;

a processor coupled to the memory;

a circuit coupled to the processor, wherein the circuit is configured to generate an ending address of data to be transferred between the memory and the processor, wherein the circuit generates the ending address from a starting address of the data to be transferred and a memory bus ~~[[data]]~~ width.

40. **(Currently Amended)** The apparatus of claim ~~[[40]]~~ 39 wherein the circuit generates an address exception when it is determined that the data to be transferred crosses a page boundary of a page in the memory.

41. **(Currently Amended)** The apparatus of claim [[40]] 39 wherein the circuit generates the ending address by:

 multiplying a stride of the data to be transferred and the memory bus [[data]] width to provide a first result;
 subtracting one from a length of the data to be transferred to provide a second result;
 multiplying the first result and the second result to provide a third result; and
 adding the third result to the starting address to provide the ending address.